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$$\begin{aligned}
 & \text{31A} \quad \text{32A} \quad \text{33A} \quad \text{34A} \\
 & \quad \quad \quad | \quad \quad | \quad \quad | \quad \quad | \\
 \text{CHA_OUT} &= \text{CHA_SOURCE} + [\text{K}_1 * (\text{CHB_SOURCE}_{\text{delayed_by_D1}})] - [\text{K}_2 * (\text{CHA_SOURCE}_{\text{delayed_by_D2}})] \\
 & \text{35A} \quad \text{36A} \quad \text{37A} \\
 & \quad \quad \quad | \quad \quad | \quad \quad | \\
 & - [\text{K}_3 * (\text{CHB_SOURCE}_{\text{delayed_by_D3}})] + [\text{K}_4 * (\text{CHA_SOURCE}_{\text{delayed_by_D4}})] + \dots
 \end{aligned}$$

Fig. 1 A

$$\begin{aligned}
 & \text{31B} \quad \text{32B} \quad \text{33B} \quad \text{34B} \\
 & \quad \quad \quad | \quad \quad | \quad \quad | \quad \quad | \\
 \text{CHB_OUT} &= \text{CHB_SOURCE} - [\text{K}_5 * (\text{CHA_SOURCE}_{\text{delayed_by_D5}})] - [\text{K}_6 * (\text{CHB_SOURCE}_{\text{delayed_by_D6}})] \\
 & \text{35B} \quad \text{36B} \quad \text{37B} \\
 & \quad \quad \quad | \quad \quad | \quad \quad | \\
 & + [\text{K}_7 * (\text{CHA_SOURCE}_{\text{delayed_by_D7}})] + [\text{K}_8 * (\text{CHB_SOURCE}_{\text{delayed_by_D8}})] - \dots
 \end{aligned}$$

Fig. 1 B

$$\begin{aligned}
 \text{SURROUND_A_OUT} &= - [\text{K}_9 * (\text{CHB_SOURCE}_{\text{delayed_by_D9}})] + [\text{K}_{10} * (\text{CHA_SOURCE}_{\text{delayed_by_D10}})] \\
 & + [\text{K}_{11} * (\text{CHB_SOURCE}_{\text{delayed_by_D11}})] - \dots
 \end{aligned}$$

FIG. 1 C

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$$\begin{aligned} \text{SURROUND_B_OUT} = & [K_{12} * (\text{CHA_SOURCE_delayed_by_D12})] + [K_{13} * (\text{CHB_SOURCE_delayed_by_D13})] \\ & - [K_{14} * (\text{CHA_SOURCE_delayed_by_D14})] - \dots \end{aligned}$$

Fig. 1D

$$\begin{aligned} \text{SURROUND_A_OUT} = & - [K_9 * ((\text{CHA_SOURCE-CHB_SOURCE})_{\text{delayed_by_D9}})] \\ & + [K_{10} * ((\text{CHA_SOURCE-CHB_SOURCE})_{\text{delayed_by_D10}})] \\ & + [K_{11} * ((\text{CHA_SOURCE-CHB_SOURCE})_{\text{delayed_by_D11}})] - \dots \end{aligned}$$

Fig. 1E

$$\begin{aligned} \text{SURROUND_B_OUT} = & + [K_{12} * ((\text{CHA_SOURCE-CHB_SOURCE})_{\text{delayed_by_D12}})] \\ & + [K_{13} * ((\text{CHA_SOURCE-CHB_SOURCE})_{\text{delayed_by_D13}})] \\ & - [K_{14} * ((\text{CHA_SOURCE-CHB_SOURCE})_{\text{delayed_by_D14}})] - \dots \end{aligned}$$

Fig. 1F

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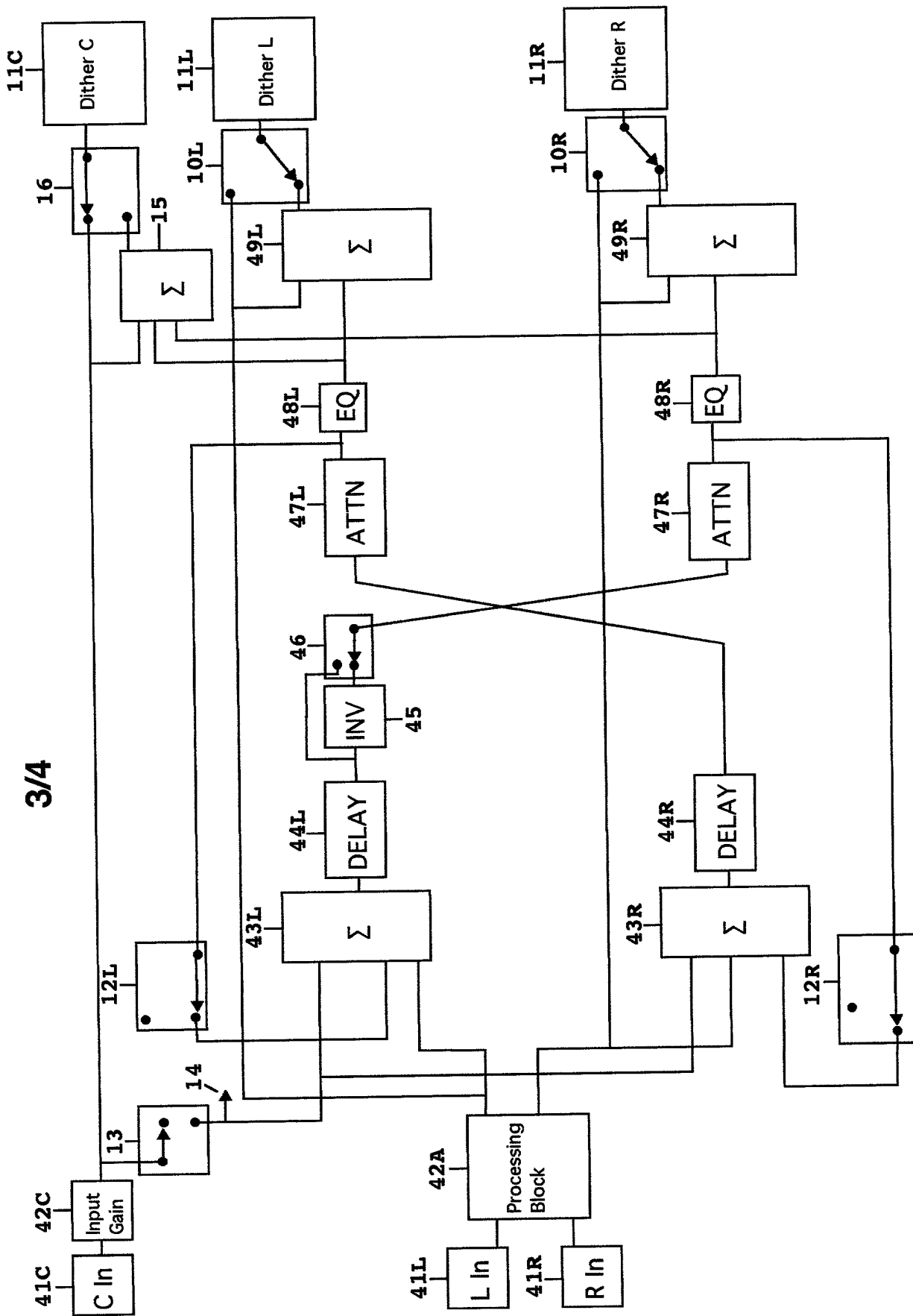


Fig. 2

FIG. 3 is a block diagram of a 4/4 stereo processing system. The system includes a 4/4 stereo input (41LS, 41RS) and a 4/4 stereo output (42LS, 42RS). The input signals are processed by input gain blocks (42LS, 42RS) and then fed into a 4/4 stereo processing block (14). The processing block includes a 4/4 stereo feed switch (17) and a 4/4 stereo feedback switch (25A, 25B). The output signals are then processed by output gain blocks (42LS, 42RS) and fed into a 4/4 stereo output block (11LS, 11RS). The system also includes a 4/4 stereo feedback path (11LFE, 11RFE) and a 4/4 stereo input gain block (42LFE, 42RFE).

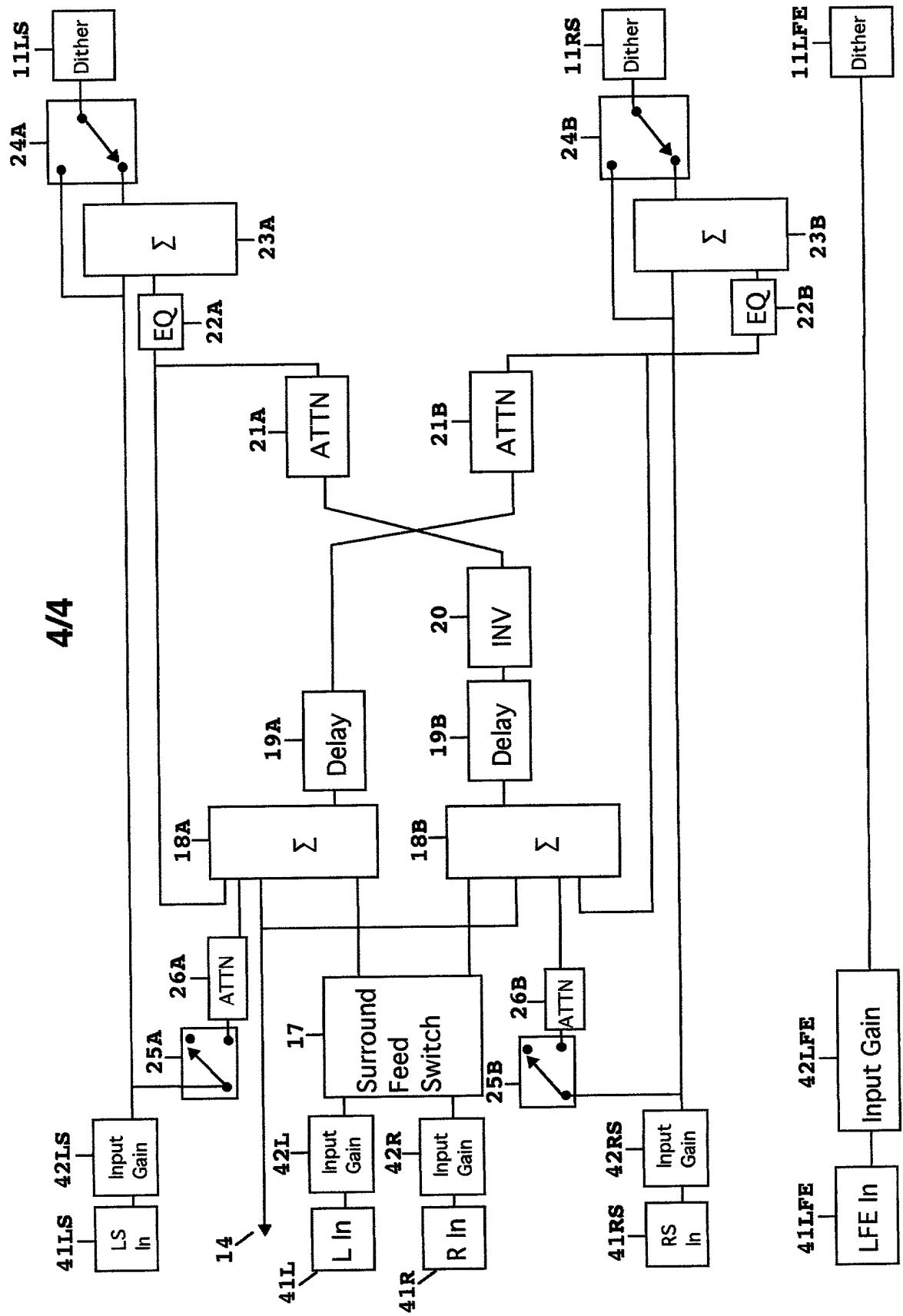


Fig. 3